Groupe de Recherche en Informatique, Image, Automatique et Instrumentation de Caen

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Université de Caen Basse-Normandie & ENSICAEN

Low frequency noise at cryogenic temperatures in state-of-the-art CMOS devices

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Context

In addition to some space applications that use cryogenic electronics, the studies at very low temperatures operation can also be of major importance for some emerging cryogenic applications of Si CMOS such as circuits for quantum computing.

Indeed, quantum computing on silicon (Si) has attracted a lot of attention because of its high potential for large-scale integration of qubits using CMOS processes. In addition, the co-integration of control circuits and CMOS qubits on a Si substrate is an ideal approach for manipulating integrated qubits. Lately, important efforts have been made to improve the coherence-time of Si qubits, and it has been revealed that low frequency charge noise is an exclusive factor limiting qubit performance. Low-frequency noise is very sensitive to traps in the gate dielectric (transistors at the control circuit) that can interfere with the operation of qubits through interconnections. Low-frequency noise can therefore be a crucial obstacle to the operation of the quantum computer on Si.

As part of the existing research collaboration with imec[1] (Leuven, Belgium), the proposed work falls within this context: rRecently, imec launched a program on the development of circuits for quantum computing. Besides the fabrication of q-bits, regular CMOS circuitry is required for the read-out of the memory. The read-out CMOS circuitry will function at liquid helium temperatures (4.2 K). This implies that the characterization of existing technology nodes at (deep) cryogenic temperatures is necessary, providing the necessary information on the suitability of FinFETs, nanowire (NW) and nanosheets (NS) FETs for such applications.

Objectifs

This goal is to carry out an in-depth DC and low-frequency noise study in a broad temperature range (from 300 K down to 4.2 K), and to extract the relevant device parameters as a function of temperature, in order to allow a better operation understanding of state-of-the-art transistors (FinFETs, GAA NW FETs, GAA NS FETs) and the possible impact of electrically active defects. The main objective will be to rely on the study at cryogenic temperatures in order to have indications concerning which technology will therefore be more appropriate to be associated with qubits for quantum computer type applications.

The first objective of the study is technological: one can use the study of the behaviour in static mode of operation and measures of low frequency noise as a non-destructive combined diagnostic tools testing for the detection of defects and errors in the process and thus to propose elements of improvement of the manufacturing processes.

The second objective is more fundamental: miniaturization and the use of new materials inevitably leads to original and unexpected physical behaviour. The study of the behaviour at low temperature may reveal new information enabling a better understanding of the charge transport and fluctuations.

The work is part of a research collaboration with imec (Leuvain, Belgium). Doctoral internships at imec will be planned.

Required skills: semiconductor physics, MOS devices operation/modeling; knowledge of low-frequency noise will be a plus.

M2 internship possible. **Thesis start: autumn 2022**. **Funding** (obtained): **RIN PhD student 100% (Normandy region funds)**

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[1]***imec*** *(https://www.imec-int.com/en/home), located in Europe, one of the world's poles of R&D and innovation in nanoelectronics and digital technologies, partner of the main manufacturers of integrated circuits and universities)*

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